Application No.: 10/728,137 Docket No.: JCLA11902

AMENDMENTS

In The Specification:

Please amend paragraph [0016] as follows:

[0016] Fig. 2 is a schematic cross-sectional view of a P-channel EEPROM undergoing a programming operation utilizing the snapback effect of a parasitic bipolar junction transistor according to this invention. As shown in Fig. 2, the P-channel EEPROM comprises an N-well 100, a floating gate 110, a control gate 120, a select gate 130, a P-type source region 140, a P-type drain region 150 and a P-doped region 160 coupled to a bit line (BL) 162~~(not shown)~~. In the programming operation, a positive voltage V_{cg} of, for example, 5V-6V is applied to the control gate 120, the N-well 100 is grounded (that is, the voltage V_b of the N-well is 0V), and a positive voltage or a programming current I_s is applied to the source region 140. The programming current I_s can be set to several nA to several μA, for example, depending on the application. It is noted that the programming current I_s can be adjusted to reach a balance point between power consumption and programming speed. In general, increasing the programming current I_s increases the programming speed, but adversely increases the power consumption. Conversely, although decreasing the programming current I_s decreases the programming speed, the overall power consumption can be reduced.

In The Drawings

Please amend FIG. 2 by adding BL 162. A replacement sheet is submitted.